ABSTRACT

A process is described for shrinking gate lengths and poly interconnects simultaneously during the fabrication of an integrated circuit. A positive tone photoresist is coated on a substrate and is first exposed with an alternating phase shift mask that has full size scattering bars which enable a gate dimension to be printed that is ¼ to ½ the size of the exposing wavelength. The substrate is then exposed using a tritone attenuated phase shift mask with a chrome blocking area to protect the shrunken gates and attenuated areas with scattering bars for shrinking the interconnect lines. Scattering bars are not printed in the photoresist pattern. The process affords higher DOF, lower OPE, and less sensitivity to lens aberrations than conventional lithography methods. A data processing flow is provided which leads to a modified GDS layout for each of the two masks. A system for producing phase shifting layout data is also included.